Dr. Lawrence A. Spracklen

Email :
Phone :
Location : Bay Area, CA.

Synopsis

10-years experience in a diverse range of key areas, spanning processor design and research, application performance analysis, software optimization and multi-thread scalability, security, hardware accelerator development, application-specific (rich media etc) instruction-set customization, video codec optimization and the development of performance primitive libraries.

Career History

September 2009 to Present
Software performance lead, Tegra Group, Nvidia

Software performance lead for a next-generation (tablet-orientated) Tegra processor. Responsible for ensuring software meets performance targets. Involved in all aspects of project performance, ranging from hands-on analysis and optimization to co-coordinating performance between the hardware, software and compiler teams.

Major Achievements:

- Architected & developed infrastructure to enable effective performance analysis and performance tracking.
- Provided feedback to the compiler team on a wide-variety of optimization opportunities for improved SPECcpu performance.
- Suggested a number of performance orientated and performance observability features adopted and integrated by hardware team.

March 2006 to September 2009
Senior Staff Engineer, Microelectronics Architecture Group, Sun Microsystems

Architect & performance analyst for UltraSPARC processors. Actively involved in defining all major components of Sun's next-generation processors (cores, caches, SoC and memory controllers) and ensuring that key software applications achieve optimum performance on the latest SPARC processors.

Major Achievements:

- Program lead for efforts investigating next-generation on-chip accelerators (security, networking, compression, XML etc.), instruction set customization (general SIMD, & Rich media acceleration), Web 2.0 performance and Java (and other managed language) acceleration.
- Architect of future-generation UltraSPARC hardware cryptographic accelerators.
- Team-lead for cross-organizational effort to improve security performance & scalability on the UltraSPARC T2 processor (e.g. IPsec, SSL, SSH, secure NFS, IDS, secure MySQL).
- Improved performance (both single- & multi-threaded) of key functions in Solaris10 (by up to 6X), ranging from cryptographic optimizations (for both software implementations and hardware offload) to bcopy and compression optimizations (SIMD and assembly language optimizations).
- Program liaison to the compiler team – driving targeted optimizations for next generation SPARC processors.
- Numerous patents pending on microarchitectural, software optimization, cryptographic and networking innovations.

August 2003 to March 2006
Staff Engineer, Advanced Processor Architecture Group, Sun Microsystems

Research into next-generation onchip accelerators & overcoming critical bottlenecks (e.g. memory wall, power constraints, bandwidth constraints) in next-generation server processors.

Major Achievements:

- Redesigned interface to UltraSPARC RF (Rainbow Falls) onchip cryptographic accelerators (presented at Hot Chips 2009).
- SPARC Microelectronics liaison to Sun Security Ambassadors.
- Designed and developed a variety of link, cache and memory compression techniques to alleviate bottlenecks in future multi-core processors.
- Developed cycle-accurate models of CMT (Chip Multithreaded) processors (including detailed memory hierarchy models and onchip hardware accelerators).
- 9 papers accepted to leading journals and conferences.

November 2000 to August 2003
Software Architect, Compilers, Libraries and Performance Technologies, Sun Microsystems

Focused on the expansion (into networking and cryptography) of Sun's SIMD Instruction Set. Video Codec acceleration and performance tuning and analysis of key customer workloads.

Major Achievements:

- Primary architect and implementer of the EEMBC (Embedded Microprocessor Benchmark Consortium) version 2 networking benchmarks.
- Primary architect of the search and sort portion of Sun's MediaLib SIMD performance library.
- Developed SPARC optimized MPEG-2 and MPEG-4 encoders and decoders (in addition to various DSP algorithms)
- Architected and modeled cryptographic instruction set extensions in next-generation SPARC processors.
- Active participant in Sun's "tunathon" efforts to tune and thread numerous ISV applications
- Selected for participation in Sun's EBoB (Engineering Best of the Best) program; a career fast-track program.
- Technical liaison between the processor design teams and the SIMD software development team.

September 2000 to November 2000
Software Engineer, Sun Microsystems

Sun SPARC performance expert for an Ericsson JIT compiler project, working onsite in Stockholm, Sweden with the Ericsson engineering team. In addition to providing advice on performance tuning, worked to ensure their design methodologies suited the UltraSPARC processor and that UltraSPARC specific enhancements were leveraged to their full potential.

Major Achievements:

- Primary technical liaison between Ericsson and Sun.

February 2000 to September 2000
Consultancy for the UN Comprehensive Test Ban Treaty Organization (CTBTO)

Designed and developed a system capable of sending, receiving and verifying the seismic data transmitted from the numerous seismic monitoring stations required to ensure treaty compliance (the data is transmitted over TCP/IP links using the International Data Center's (IDC) Continuous Data (CD1) protocol). This system, which is a multithreaded implementation for Solaris and Linux systems, has been used by the CTBTO to determine the compliance of the monitoring stations before they 'go-live'.

Major Achievements:

- Designed, managed, implemented and documented the 50K line C-based development.

February 1997 to May 1997
Graduate Student Intern, Sun Microsystems

Worked on optimizing a large multithreaded, multiprocessor, networking benchmark for a telecommunications customer.

Major Achievements:

- Re-implemented the benchmark using lock-free synchronization, significantly improving performance.

February 1996 to May 1996
Graduate Student Intern, Sun Microsystems

Researched the feasibility of using Sun's VIS SIMD instructions to accelerate key network protocols.

Major Achievements:

- Developed (and patented) novel technique to accelerate TCP checksum computations.

February 1996 to February 2000

Ph.D. in the Electrical Engineering funded by Sun Microsystems

Researched the feasibility of utilizing SIMD instruction set extensions to accelerate important communications, network and cryptographic protocols. Research focused on devising microarchitecture enhancements that could be included in future releases of Sun's UltraSPARC processor in order to improve performance of key protocols.

Major Achievements:

- Teaching assistant for the final year processor design course.
- Sun patented several key concepts of the Ph.D.
- Gave research presentations to many companies including; Ericsson, Elsag Bailey, Alcatel, Telesoft, Data Kinetics.

Thesis Title: "SIMD Systems and Communications Applications"

Education and Qualifications

February 1996 to February 2000

Doctor of Philosophy, Electrical Engineering, University of Aberdeen

October 1992 to July 1995

B.Sc. with First Class Honors in Computational Physics, University of York

Honors Project: "Image recognition using Kohonen Feature Map Techniques".

Software Development Experience

- Extensive use of C and a working knowledge of Python, C++, Java, FORTRAN and Perl.
- Comprehensive experience with assembly language programming.
- Extensive knowledge of software optimization techniques.
- Bash scripting skills

Recent Publications

2009

* J. Hughes, G. Morton, J. Pechanec, C. Schuba, L. Spracklen and B. Yenduri, "Transparent Multicore Cryptographic Support on Niagara CMT Processors", in IEEE International Workshop on Multicore Software Engineering, May 2009.

* L. Spracklen. "Maximizing Multicore Memory Bandwidth Using Compression", presented at Multicore Expo, March 2009.

2008

* M. Thuresson, L. Spracklen and P. Stenstrom. "Memory-Link Compression Schemes: A Value Locality Perspective", in IEEE Transactions on Computers, Vol. 57, No. 7, July 2008.

* L. Spracklen. "Multicore Processors and Microparallelism", presented at Sun Community One Conference, May 2008.

* L. Spracklen. "Multicore Processors and Microparallelism", presented at Multicore Expo, April 2008.

2007

* M. Shah, J. Barreh, J. Brooks, R. Golla, G. Grohoski, N. Gura, R. Hetherington, P. Jordan, M. Luttrell, C. Olson, B. Saha, D. Sheahan, L. Spracklen and A. Wynn, "UltraSPARC T2: A Highly-Threaded, Power-Efficient, SPARC SOC", in Proceedings of the IEEE Asian Solid-State Circuits Conference, November 2007.

* J. Laudon and L. Spracklen. "The Coming Wave of Multithreaded Chip Multiprocessors", in International Journal of Parallel Programming, Vol. 35, No. 3, pp. 299-330, June 2007.

* D. Gove and L. Spracklen, "Evaluating the correspondence between training and reference workloads in SPEC CPU2006", in ACM Computer Architecture News, Vol. 35, No. 1, pp.122-129, 2007.

2006

* D. Gove and L. Spracklen, "Evaluating whether the training data provided for profile feedback is a realistic

control flow for the real workload", in Proceedings of the SPEC Benchmark Workshop, January 2006.

2005

* H.Eberle, S. Chang Shantz, V. Gupta, N. Gura, L. Rarick and L. Spracklen. "Accelerating Next-Generation Public-Key Cryptosystems On General-Purpose CPUs", in IEEE Micro, Vol. 25, No. 2, pp. 52-59, 2005.
* Y. Chou, L. Spracklen and S. G. Abraham, "Store Memory-Level Parallelism Optimizations for Commercial Applications", in Proceedings of the IEEE/ACM International Symposium on Microarchitecture, November 2005.
* H. Modi, L. Spracklen, Y. Chou and S. G. Abraham, "Accurate Modeling of Aggressive Speculation in Modern Microprocessor Architectures", in Proceedings of the IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, September 2005.
* L. Spracklen, Y. Chou and S. G. Abraham. "Effective Instruction Prefetching in Chip Multiprocessors", in Proceedings of the 11th International Symposium on High-Performance Computer Architecture, February 2005.
* L. Spracklen and S. G. Abraham, "Chip Multithreading: Opportunities and Challenges", in Proceedings of the 11th International Symposium on High-Performance Computer Architecture, February 2005.

2004

* S. Iacobovici, L. Spracklen, S. Kadambi, Y. Chou and S. Abraham. "Effective Stream-Based and Execution-Based Data Prefetching", in Proceedings of the 18th Annual ACM International Conference on Supercomputing, June 2004.

Professional Recognition

Member of the program committee for the IEEE International Conference on Computer Design, ACM International Conference on Supercomputing, IEEE International Symposium on Workload Characterization, IEEE International Symposium on Performance Analysis of Systems and Software, and IEEE Workshop on Interaction between Compliers and Computer Architectures.

Patents

11 granted US patents (US5960012, US7003653, US7013377, US7373482, US7434004, US7434031, US7480787, US7529911, US7543112, US7599489, US7650374), 20+ US patents pending (or soon to be filed)